

CCA

MR-50P		
33	* AB2X	01 * AB1X
34	* AB4X	02 * AB3X
35	* AB7X	03 * AB5X
36	* A10X	04 * AB8X
37	* A13X	05 * A11X
38	* A16X	06 * A14X
39	* BAUDR	07 BV
40	* CLK0	08 BV
41	-15V	09 BV
42	BV	10 +5V
43	+24V	11 +5V
44	EXRDY	12 +5V
45	D02X	13 D01X
46	D05X	14 D03X
47		15 D06X
48		16
49		17
50		18

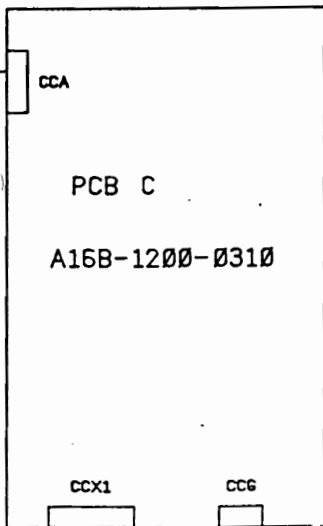
CCX1

MR-50P		
33		01 TTY1
34	RS	02 TTY2
35	CS	03 TTY3
36	DR	04 OV
37	OV	05
38	* CD	06
39	OV	07 PR
40	* SD	08 TE
41	* RD	09 ERR
42	OV	10 +6V
43	ER	11 CH01
44		12 CH02
45		13 CH03
46	SD	14 CH04
47	OV	15 CH05
48	CH09	16 CH06
49	PI	17 CH07
50	FG	18 CH08

CCG

MR-20P		
14	SLH	08 D000
15	* SLH	09 * D000
16	SLL	10 ORH
17	* SLL	11 * ORH
18	BV	12 D06
19	BV	13 * D06
20	FG	01 D003
		02 * D003
		03 D002
		04 * D002
		05 D001
		06 * D001
		07 BV

MASTER PCB (MODEL-B)



TO CRT (GRAPHIC) DISPLAY UNIT

C14

MR-20P		
14	CH4	01 PR
15	CH5	02 TE
16	CH6	03 ERR
17	CH7	04 TTY3
18	CH8	05 +6V
19	CH9	06 TTY2
20	PI	07 TTY1

ASR33.FACIT4070 INTERFACE

C15

DSUB-25S

01	FG	14	
02	* SD	15	
03	* RD	16	
04	RS	17	
05	CS	18	
06	DR	19	
07	OV	20	ER
08	* CD	21	
09		22	
10		23	
11		24	
12		25	+24V
13			

RS-232C INTERFACE

CJ01

14	13	12	11	10	9	8
14 PIN IC						
1	2	3	4	5	6	7

			14 INCH COLOR GRAPHIC INTERFACE	
			A16C-1200-0310/01~	

MAIN CPU DI/DO (SYSTEM 6)

	D7	D6	D5	D4	D3	D2	D1	D0
BE7EE (DI)	* CRT/P	* GRC/P	* 14/9	IRM	DOG	* CR9		FACIT

* CRT/P --- = $\bar{1}$ WITH CRT/PUNCH CONTROL P.C.B.
 * GRC/P --- = $\bar{1}$ WITH GRAPHIC/PUNCH CONTROL P.C.B.
 FACIT --- = $\bar{1}$ FACIT 487B IS CONNECTED.
 IRM --- = $\bar{1}$ INPUT READY (FIFO IS NOT FULL)
 DOG --- GRAPHIC CPU DO
 * CR9 --- = $\bar{1}$ WITH 9 INCH CRT = $\bar{1}$ WITH 12 INCH CRT
 * 14/9 --- = $\bar{1}$ WITH 12 INCH CRT = $\bar{1}$ WITH 9 OR 12 INCH CRT

	D7	D6	D5	D4	D3	D2	D1	D0
BE7F8 (DI/DO)	P7	P6	P5	P4	P3	P2	P1	P0

P8-P7 --- ASR33,RS-232C DATA(DI/DO)
 FACIT 487B DATA(DO)

	D7	D6	D5	D4	D3	D2	D1	D0
BE7F2 (DI/DO)	S7	S6	S5	S4	S3	S2	S1	S0

ERR --- ERROR OF FACIT 487B SIDE
 TE --- PAPER TAPE END (FACIT 487B)
 PB --- PUNCH BUSY (FACIT 487B)
 P1 --- PUNCH INSTRUCTION (FACIT 487B)

	D7	D6	D5	D4	D3	D2	D1	D0
BE7F4 (DO)	CLDCD	PINH	FA/ASRS	RS/AS			SY3/SY6	5MHZ

CLDCD --- = $\bar{1}$ → 1 → $\bar{1}$ CLEAR DCD HOLD SIGNAL
 PINH --- = $\bar{1}$ PUNCH INHIBIT

FA/ASRS,RS/AS	FACIT 487B	ASR33	RS-232C
FA/ASRS	1	0	0
RS/AS	0 OR 1	0	1

SY3/SY6 --- = $\bar{1}$ SYSTEM 3 = $\bar{1}$ SYSTEM 6
 5MHZ --- = $\bar{1}$ MAIN CLOCK FREQ. IS 5MHZ.

	D7	D6	D5	D4	D3	D2	D1	D0
BE7F6 (DI)					DCD			

DCD --- = $\bar{1}$ DATA (FROM RS-232C INTERFACE) IS NOT GOOD.

	D7	D6	D5	D4	D3	D2	D1	D0
BE7FC (DI/DO)	GCD7	GCD6	GCD5	GCD4	GCD3	GCD2	GCD1	GCD0

GCD8 --- DO MAIN CPU → GRAPHIC CPU

MAIN CPU DI/DO (SYSTEM 3)

	D7	D6	D5	D4	D3	D2	D1	D0
BE7EC (DI)						= GRC/P		

* GRC/P --- = $\bar{1}$ WITH GRAPHIC/PUNCH CONTROL P.C.B.

	D7	D6	D5	D4	D3	D2	D1	D0
BE7FA (DO)							SY3/SY6	

SY3/SY6 --- = $\bar{1}$ SYSTEM 3 = $\bar{1}$ SYSTEM 6

	D7	D6	D5	D4	D3	D2	D1	D0
BE7F6 (DI)				IRM				DOG

IRM --- = $\bar{1}$ INPUT READY (FIFO IS NOT FULL)
 DOG --- GRAPHIC CPU DO

	D7	D6	D5	D4	D3	D2	D1	D0
BE7FC (DI/DO)	GCD7	GCD6	GCD5	GCD4	GCD3	GCD2	GCD1	GCD0

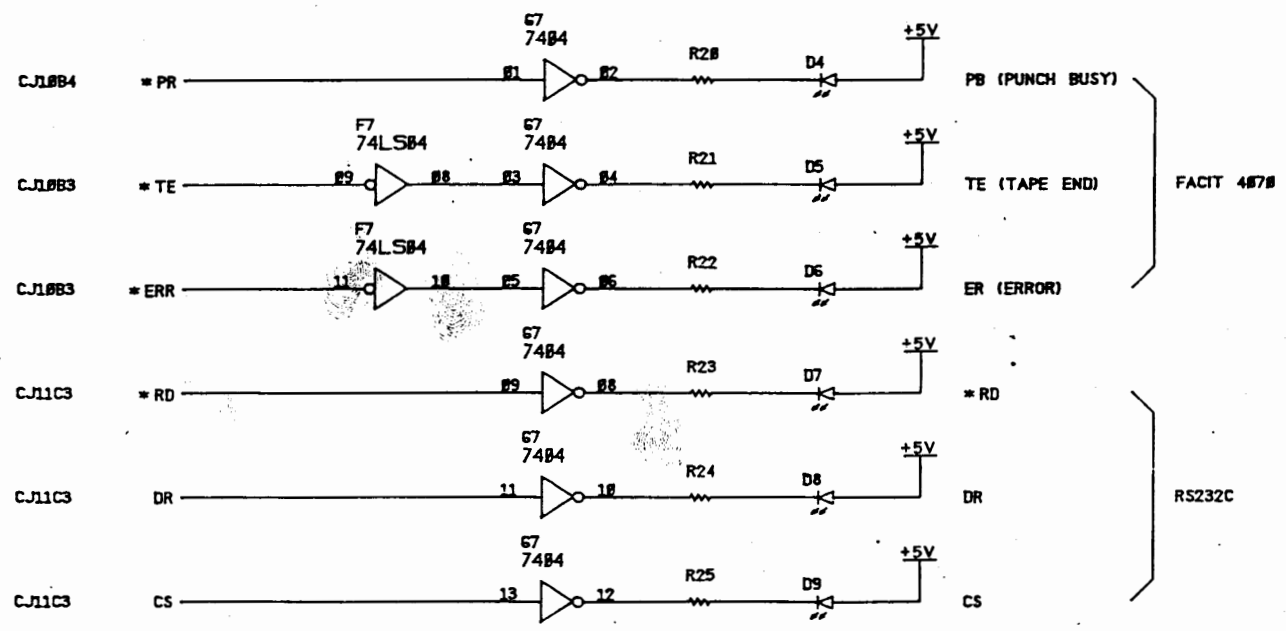
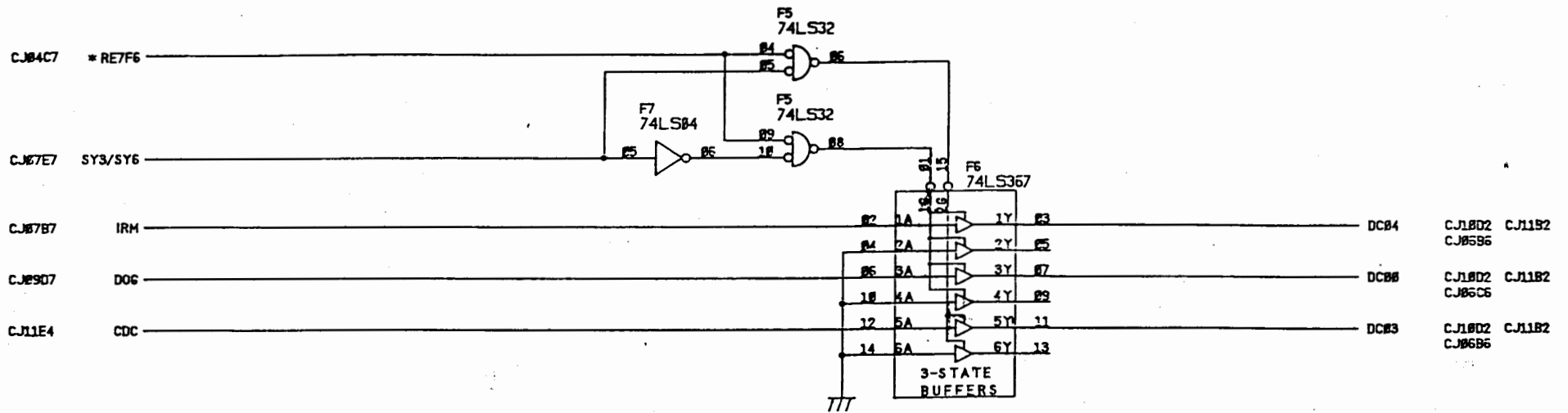
GCD8 --- DO MAIN CPU → GRAPHIC CPU

CJ02

117
445

	FILE

A16C-1200-0310/01

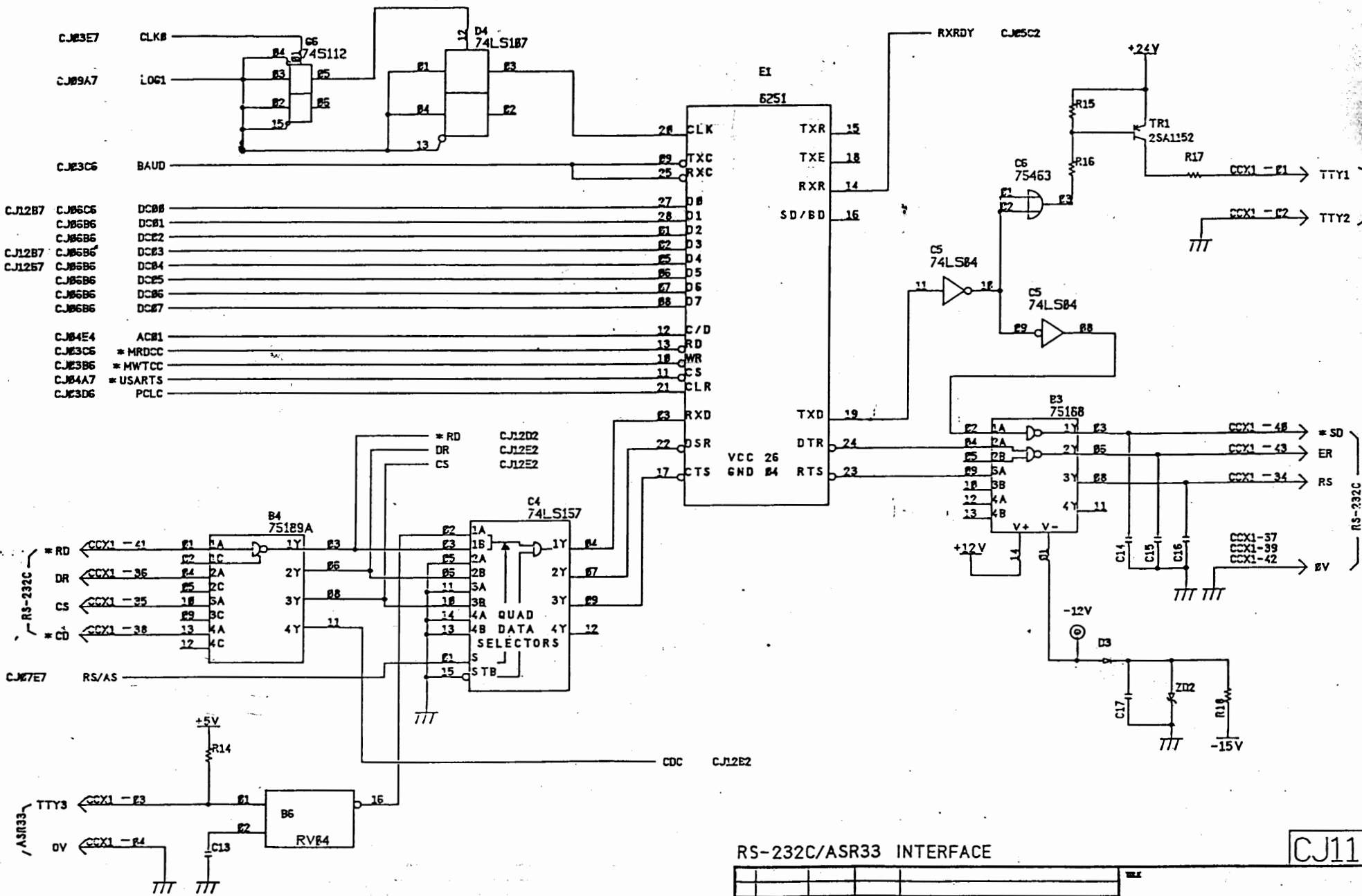


FACIT.RS-232C SIGNAL DISPLAY

CJ12

						A16C-1200-0310/01	

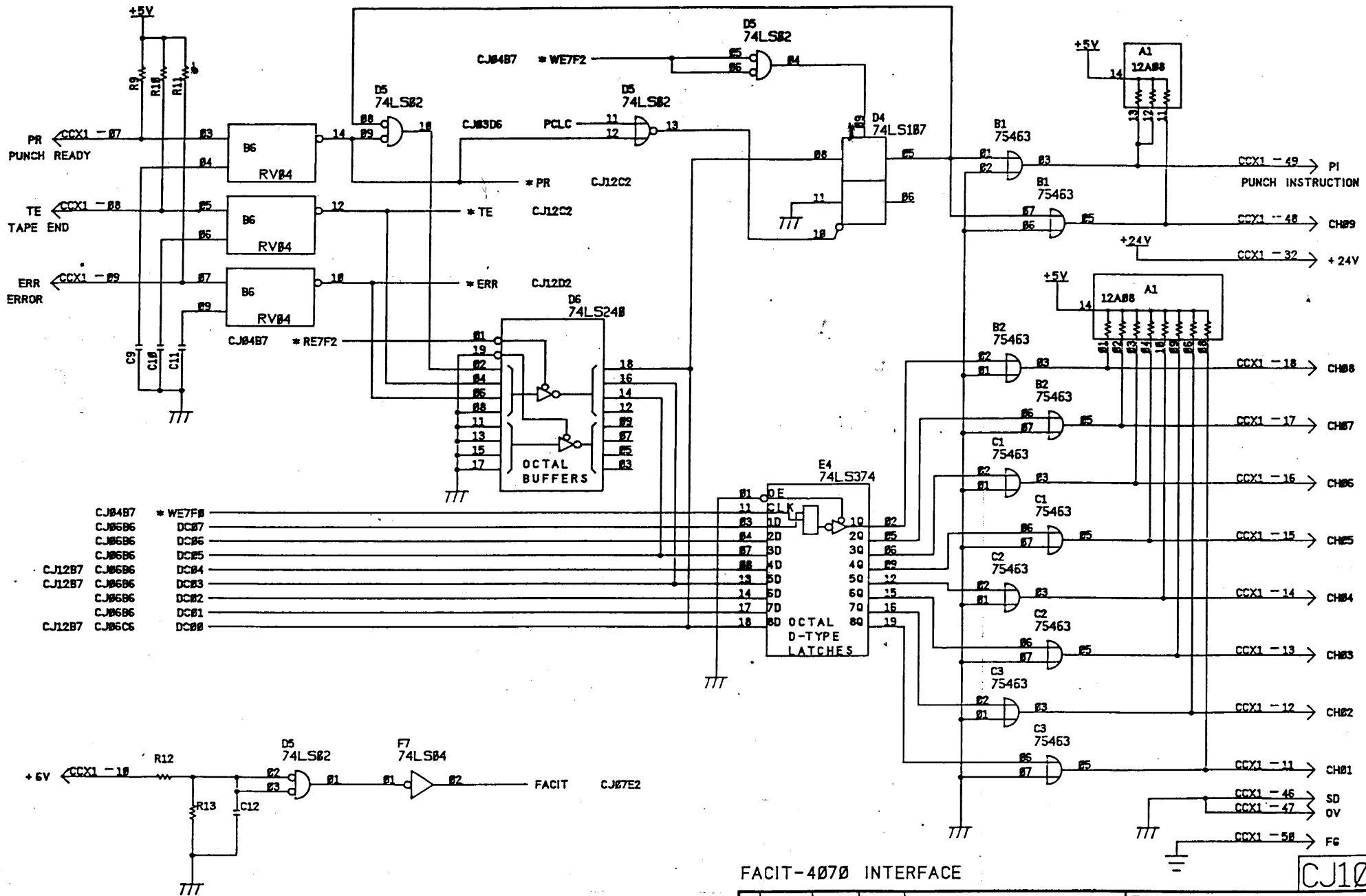
127
123
F



RS-232C/ASR33 INTERFACE CJ11

REV	REV	REV	REV	REV	REV	REV	REV	REV	REV
DRAWING NO. A16C-1200-0310/01								DATE	
FANUK LTD									

126
147
44



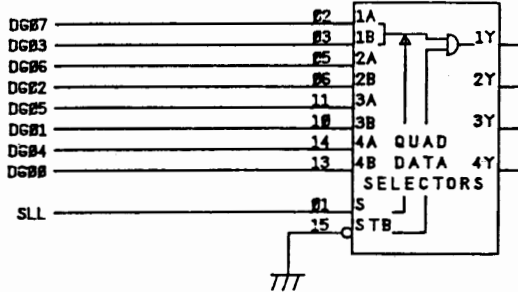
FACIT-4070 INTERFACE

CJ10

DATE		
REV. NO.		
PART NO.		A16C-1200-0310/01

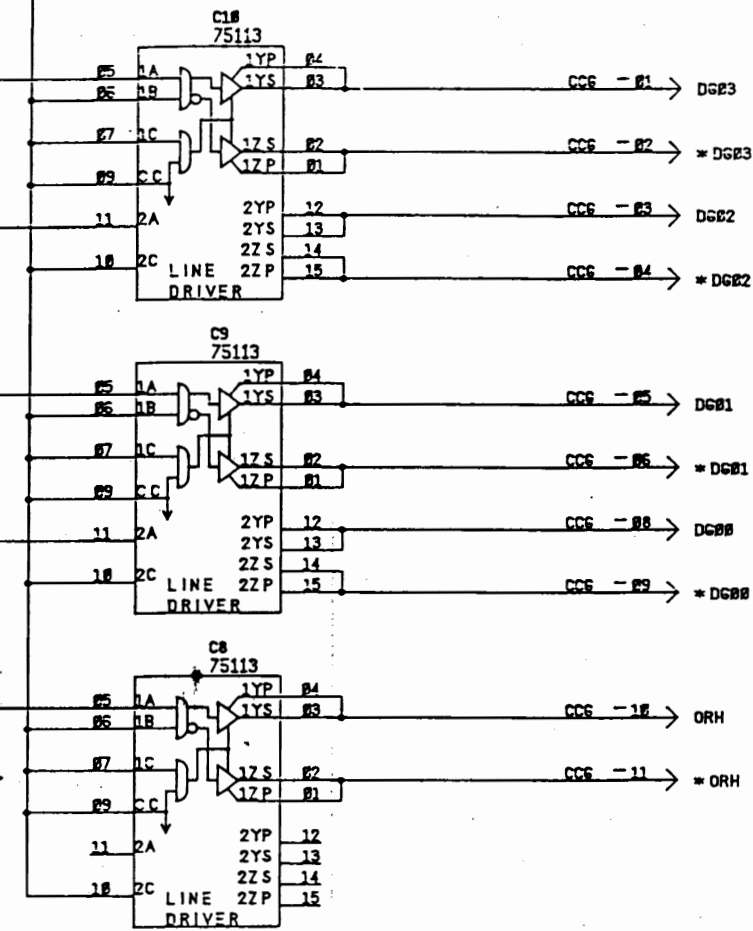
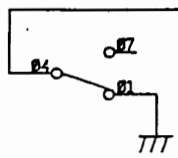
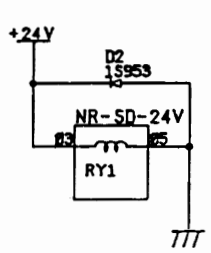
125
121
F

CJ87A7
 D687
 D683
 D686
 D682
 D685
 D681
 D684
 D688
 CJ89B7



CJ87A7

ORH



FIFO DATA DRIVER

CJ08

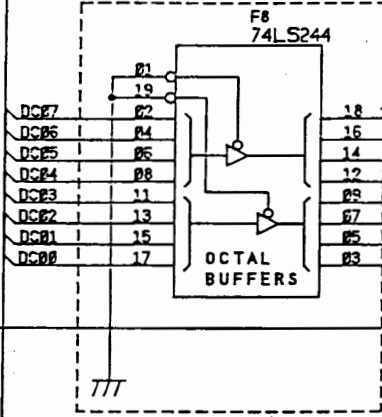
REV. 0

A16C-1200-0310/01

173
 149

NOTE DC86-DC87

CJ84E7 WFIFOM
CJ85C6 DMWTCC
CJ89B7 * SLH



CJ89C7 * SLL

02~EDITION ONLY

CJ83D6 * PCLC

CJ84E7 * WE7F4

CJ84C7 * RE7EE

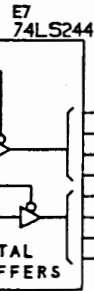
CJ89A2 LOG1

CJ87B7 IRM

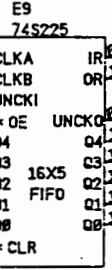
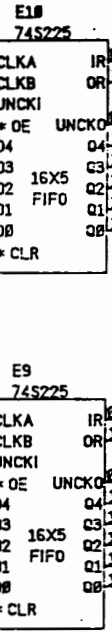
CJ8907 IOC

CJ18E4 FACIT

TTT



02~EDITION ONLY



OUTPUT READY (FIFO IS NOT EMPTY) ORH

INPUT READY (FIFO IS NOT FULL) IRM

FIFO (FIRST-IN FIRST-OUT)

CJ88D2

CJ88B2

CJ88B2

CJ88B2

CJ88C2

CJ12B2 CJ67D2

CJ88B2

CJ88B2

CJ88C2

CJ88C2

CJ84C2

CJ84C2

CJ11D1

CJ84A4

CJ84C2

CJ84C2

CJ11D1

CJ84A4

CJ85E2

CJ12B2

CJ07

REV

REV

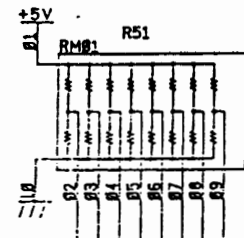
A16C-1200-0310/01

120
118

CJ0586 GPCBR
CJ0505 *MRDWT

DB7X XCCA - 31
DB5X XCCA - 15
DB5X XCCA - 45
DB4X XCCA - 32
DB4X XCCA - 14
DB3X XCCA - 45
DB2X XCCA - 15
DB1X XCCA - 15
DB0X XCCA - 28

K2
74LS245



OCTAL BUS TRAN-CEIVERS

DC07 CJ07A2 CJ1002 CJ11B2
DC06 CJ07A2 CJ1002 CJ11B2
DC05 CJ07A2 CJ1002 CJ11B2
DC04 CJ07A2 CJ1002 CJ11B2 CJ12B7
DC03 CJ07A2 CJ1002 CJ11B2 CJ12B7
DC02 CJ07A2 CJ1002 CJ11B2
DC01 CJ07A2 CJ1002 CJ11B2
DC00 CJ07A2 CJ1002 CJ11B2 CJ12B7

CJ0401 REEX-FX
CJ0407 AC04

CJ0408 0005
CJ0407 0001

CJ0409 0001
CJ0407 0001
CJ07E1 0001

H5
74S138

*RETEC

K3
74LS367

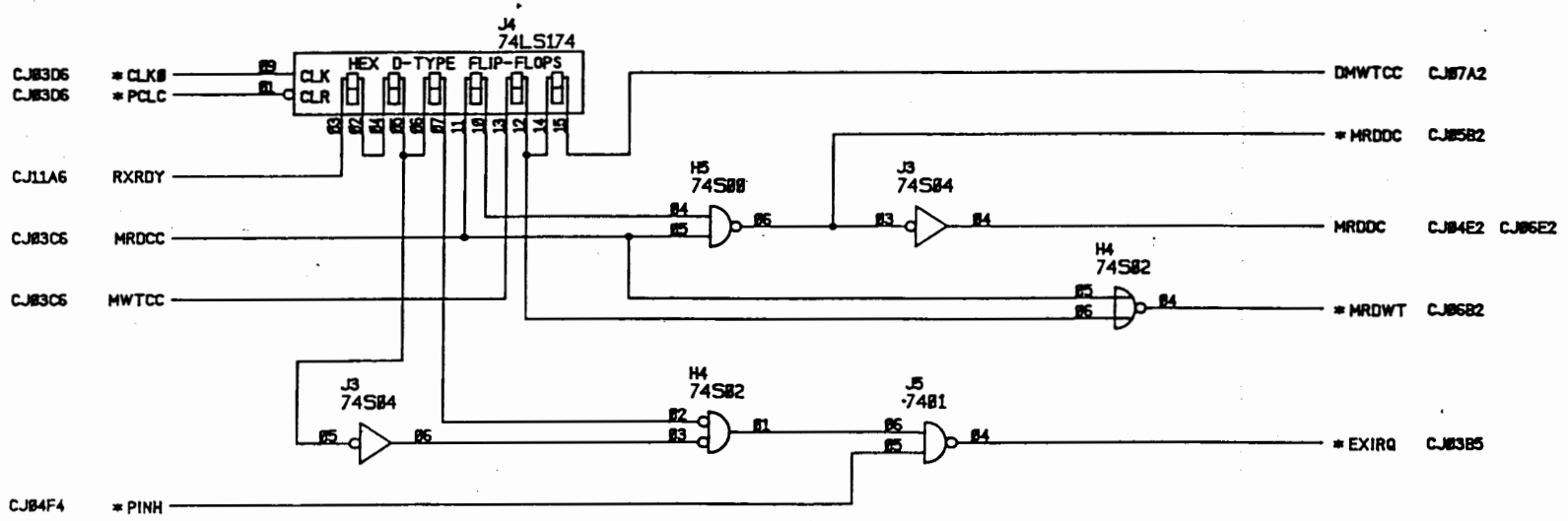
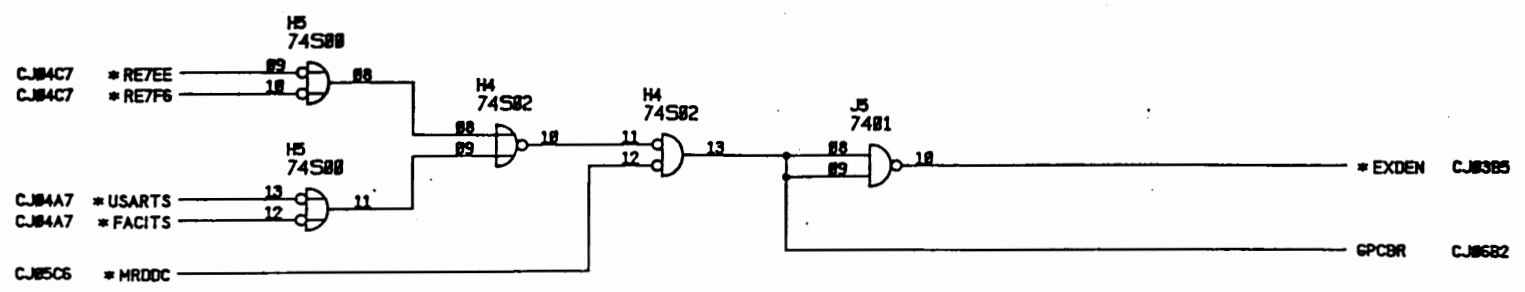
1 OF 3 DECODER

3-STATE BUFFERS

DATA BUFFER

CJ06				
PART NO. A16C-1200-0310/ 01				
REV.	DATE	BY	CHKD	DESCRIPTION

121
1/7



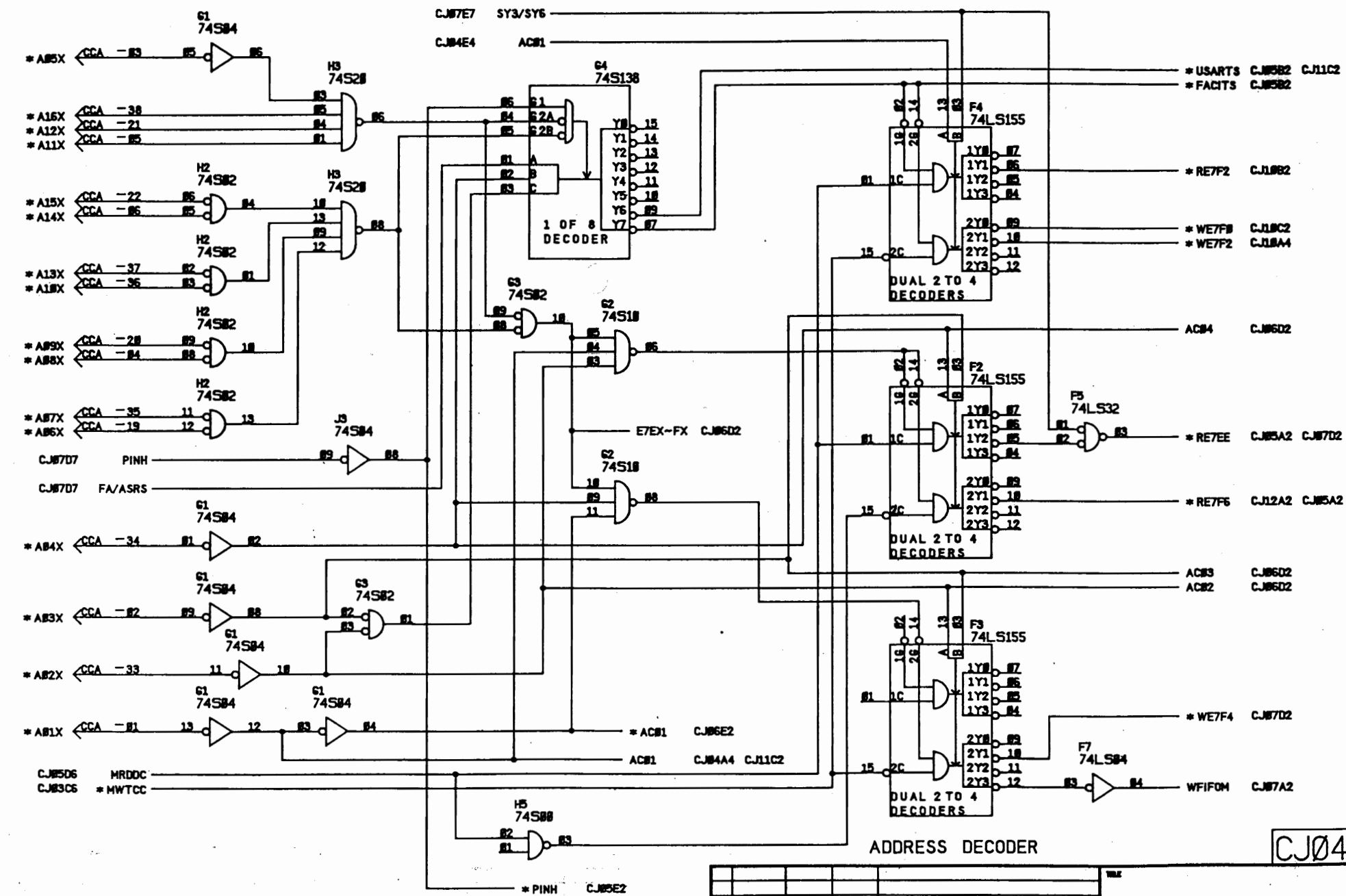
READ/WRITE SIGNAL CONTROL

CJ05

REV. NO.	
A16C-1200-0310/ 01	

100
46

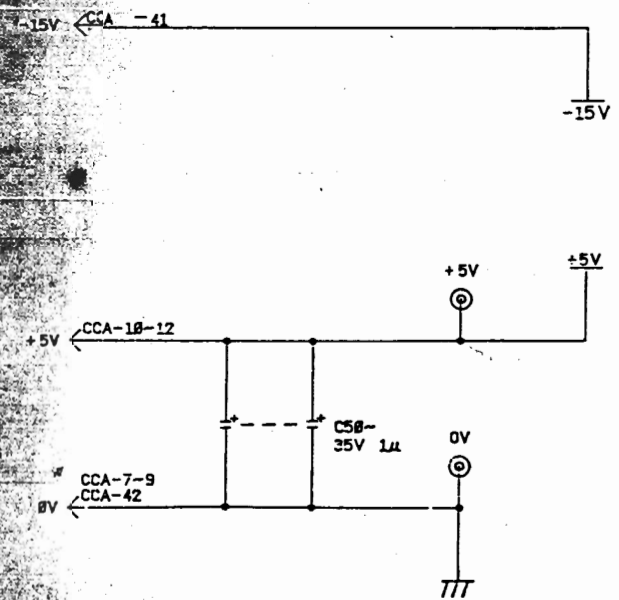
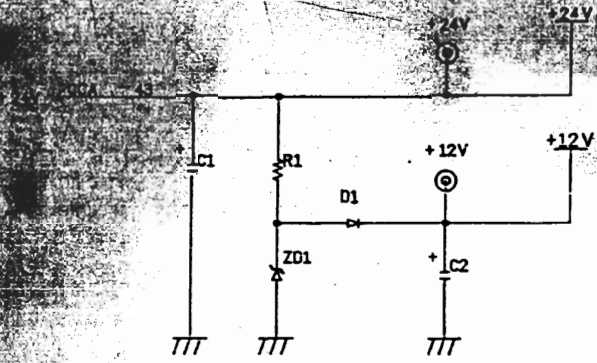
A
B
C
D
E



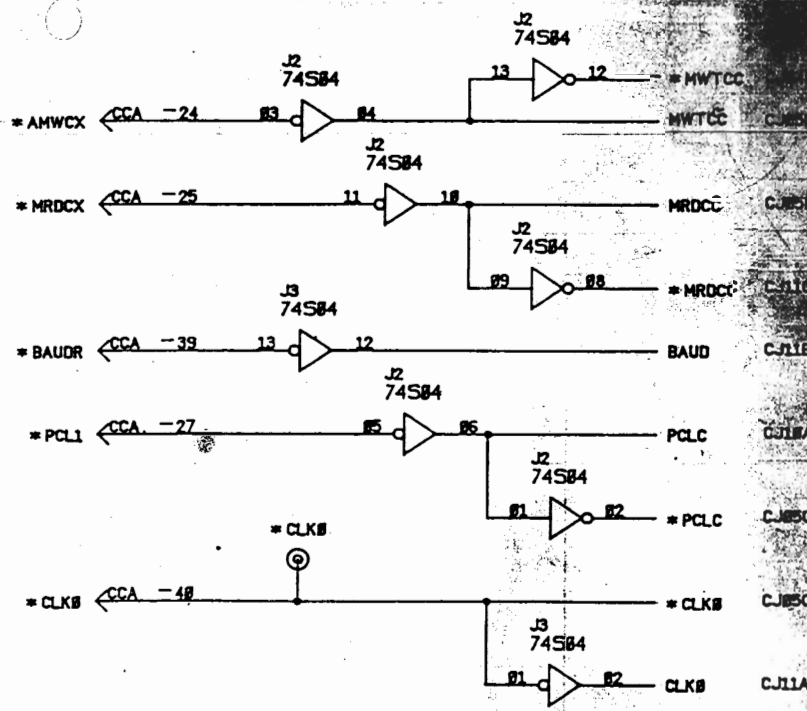
CJ04

REV
A16C-1200-0310/01

119



C-1005 = EXIRQ
 C-1006 = EXDEN



C-1002
 C-1012
 C-1102
 C-1162
 C-11A4
 C-11C2
 C-11D2
 C-11A2

MASTER P.C.B. INTERFACE

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